EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S 3	0	(image\$1 drawing\$1) SAME instruction\$1 SAME (description NEAR1 language) SAME attribute\$1 SAME color\$1 SAME memory SAME status NEAR1 flag\$1	US-PGPUB; USPAT; JPO; DERWENT	OR	ON	2007/08/08 14:02
S13	4	S12 and @ad<"20020913"	US-PGPUB; USPAT; JPO; DERWENT	OR	ON	2007/08/08 14:09
S62	0	("2002/0132665").URPN.	USPAT	OR	ON	2007/08/08 14:50
S64	2739	S63 and (@ad<"20020913" or @rlad<"20020913")	US-PGPUB; USPAT; JPO; DERWENT	OR	ON	2007/08/08 15:29
S63	3984	image\$1 and (drawing\$1 with instruction\$1)	US-PGPUB; USPAT; JPO; DERWENT	OR	ON	2007/08/08 15:29
S67	25	S65 and (pattern\$1)	US-PGPUB; USPAT; JPO; DERWENT	OR	ON	2007/08/08 15:32
S66	1186	S64 and (pattern)	US-PGPUB; USPAT; JPO; DERWENT	OR	ON	2007/08/08 15:32
S68	279682	(graphical drawing instruction).CLM.	US-PGPUB; USPAT; JPO; DERWENT	OR	ON	2007/08/08 16:58
S65	54	S64 and ((valid or invalid) NEAR4 instruction\$1)	US-PGPUB; USPAT; JPO; DERWENT	OR	ON	2007/08/08 16:58
S69	182169	S68 and (@ad<"20020913" or @rlad<"20020913")	US-PGPUB; USPAT; JPO; DERWENT	OR	ON	2007/08/08 16:59
S70	3216	S69 and ((valid or invalid) NEAR3 instruction\$1)	US-PGPUB; USPAT; JPO; DERWENT	OR	ON	2007/08/08 17:34
S72	662	S70 and image\$1	US-PGPUB; USPAT; JPO; DERWENT	OR	ON	2007/08/08 17:36

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S71	1704	S70 and (omit\$3 or skip\$3 or	US-PGPUB;	OR	ON	2007/08/08 17:36
3/1	1704	ignore\$1)	USPAT; JPO; DERWENT	OK	ON	2007/08/08 17.38
S74	7	S73 and (logical NEAR2 sum)	US-PGPUB; USPAT; JPO; DERWENT	OR	ON	2007/08/08 17:38
S73	687	S70 and (image or imag\$4)	US-PGPUB; USPAT; JPO; DERWENT	OR	ON	2007/08/08 17:40
S60	2155	S59 and (@ad<"20020913" or @rlad<"20020913")	US-PGPUB; USPAT; JPO; DERWENT	OR	ON	2007/08/13 16:55
S59	3169	image\$1 SAME drawing\$1 SAME instruction\$1	US-PGPUB; USPAT; JPO; DERWENT	OR	ON	2007/08/13 16:55
L2	661	L1 and (@ad<"20020913" or @rlad<"20020913")	US-PGPUB; USPAT; JPO; DERWENT	OR	ON	2007/08/13 16:55
L1	1061	(715/517).CCLS.	US-PGPUB; USPAT; JPO; DERWENT	OR	OFF	2007/08/13 16:55
S61	24	S60 and ((valid or invalid) NEAR4 instruction\$1)	US-PGPUB; USPAT; JPO; DERWENT	OR	ON	2007/08/13 16:56
L4	0	L3 and ((valid or invalid) NEAR4 instruction\$1)	US-PGPUB; USPAT; JPO; DERWENT	OR	ON	2007/08/13 16:56
L3	327	L2 and (image\$1 and drawing\$1 and instruction\$1)	US-PGPUB; USPAT; JPO; DERWENT	OR	ON	2007/08/13 16:56

8/13/2007 4:59:08 PM C:\Documents and Settings\jdebrow\My Documents\EAST\Workspaces\10661320.wsp Page 2



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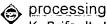
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Data cache management on EPIC architecture: optimizing memory access for image



K. Brifault, H. P. Charles

September 2003 ACM SIGARCH Computer Architecture News, Proceedings of the 2003 workshop on MEmory performance: DEaling with Applications, systems and architecture MEDEA '03, Volume 32 Issue 3

Publisher: ACM Press

Full text available: pdf(261.21 KB) Additional Information: full citation, abstract, references

Nowadays, multimedia applications are more and more used, and take a larger place in the workloads of modern computing systems. It appears that the classical 1D spatial locality arrangement in the cache is not adapted to the management of this data type, because its structures exhibit an intrinsic 2D locality. In this article, we study cache behavior and alternative strategies for multimedia, using a JPEG benchmark on an Itanium2™ cache system. We demonstrate, through systematic experiments ...

² A special purpose LSI processor using the DDA algorithm for image transformation



Katsura Kawakami, Shigeo Shimazaki

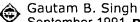
January 1984 ACM SIGARCH Computer Architecture News, Proceedings of the 11th annual international symposium on Computer architecture ISCA '84, Volume 12 Issue 3

Publisher: ACM Press

Full text available: pdf(772.26 KB) Additional Information: full citation, abstract, references, index terms

A new special purpose processor, named MN8614, has been developed for the high speed execution of binary image transformations. The processor carrys out the processing based on a new extension of the DDA algorithm to reduce the number of multiplications required for image processing. In addition, a machine instruction set has been developed which makes optimal use of the new method. The processor is fabricated on a single LSI chip with 16-bit data paths. Although the basic chip design is th ...

GRIP: graphics reduced instruction processor



September 1991 Proceedings of the 24th annual international symposium on Microarchitecture MICRO 24

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